10105617 9

Claims 1-69 (Canceled).

70. (Currently Amended): A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and having second portions projecting outwardly from the semiconductive material to a respective upper planar surface, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area of the semiconductive material therebetween, the active area of the semiconductive material having an upper planar surface extending between the first portion opposing sides, each of the opposing sides of the first portions comprising a straight segment which is normal relative to the active area upper planar surface, each of the opposing sides of the second portions comprising a straight segment which is normal relative to the active area upper planar surface, the straight opposing segments of the second portions being displaced laterally relative to the straight opposing segments of the first portions and thereby defining opposing straight step surfaces of the pair of masses extending between the respective straight segments of the first and second portions, the opposing straight step surfaces being normal each of the respective straight segments of the first and second portions, the opposing straight step surfaces being elevationally aligned with and extending from the active area upper planar surface to a respective one of the straight segments of the second portions, each of the straight

s gm nts of th second portions extending from a respective one of the straight step surfaces to a respective top upper planar surface of th STI masses;

a first gate dielectric layer received over the upper planar surface of the active area and over the step surfaces of the pair of masses, the first gate dielectric layer having upper surface portions received over the step surfaces and which are parallel with the active area upper planar surface;

a floating gate received over the first gate dielectric layer;

a second gate dielectric layer received over the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate.

71. (Previously Presented): The floating gate transistor of claim 70 wherein the first gate dielectric layer includes straight laterally outermost surfaces which bear against the straight segments of the second portions, and are thereby each normal to the active area upper planar surface.

72. (Previously Presented): The floating gate transistor of claim 70 wherein the opposing sides of the second portions define a region therebetween, the floating gate only partially filling the region.

73. (Previously Present d): The floating gate transistor of claim 70 wher in the opposing sides of the second portions define a region therebetween, the floating gate completely filling the region.

74. (Previously Presented): The floating gate transistor of claim 70 wherein the floating gate comprises a roughened uppermost surface.

75. (Previously Presented): The floating gate transistor of claim 70 wherein the opposing sides of the second portions define a region therebetween, the floating gate only partially filling the region and comprising an essentially concave uppermost surface.

76. (Previously Presented): The floating gate transistor of claim 70 wherein the opposing sides of the second portions define a region therebetween, the floating gate completely filling the region and comprising an essentially concave uppermost surface.

77. (Previously Presented): The floating gate transistor of claim 70 wherein the first dielectric layer comprises a silicon oxide.

78. (Previously Presented): The floating gate transistor of claim 70 wherein the second dielectric layer comprises a silicon oxide.

79. (Previously Presented): The floating gate transistor of claim 70 wherein the first di lectric layer and the second dielectric layer each comprises a silicon oxide.

80. (Previously Presented): The floating gate transistor of claim 70 wherein the first dielectric layer comprises ONO.

81. (Previously Presented): The floating gate transistor of claim 70 wherein the second dielectric layer comprises ONO.

82. (Previously Presented): The floating gate transistor of claim 70 wherein the first dielectric layer and the second dielectric layer each comprises ONO.

83. (Previously Presented): The floating gate transistor of claim 70 wherein the floating gate comprises hemispherical grain polysilicon.

84. (Previously Presented): The floating gate transistor of claim 70 wherein the isolation masses each comprise a silicon oxide.